Cross-References to Related Applications

This is a continuation-in-part of U. S. Serial Nos. 08/841,409, 08/837,702 and 08/837,714 all filed on April 22, 1997. Further, the following U. S. patent applications filed concurrently herewith Serial No. 09/034,687, entitled "Digital Isolation System With Data Scrambling" by Andrew W. Krone et al.; Serial No. 09/034,456, entitled "Digital Isolation With ADC Offset Calibration" by Andrew W. Krone et al.; Serial No. 09/034,455, entitled "Ring-Detect Interface Circuitry and Method for a Communication System" by Timothy J. Dupuis et al.; Serial No. 09/035,779, entitled "Call Progress Monitor Circuitry and Method for a Communication System" by Timothy J. Dupuis et al.; Serial No. 09/034,683, entitled "External Resistor and Method to Minimize Power Dissipation in DC Holding Circuitry for a Communication System" by Jeffrey W. Scott et al.; Serial No. 09/034,682, entitled "Framed Delta Sigma Data With Unlikely Delta Sigma Data Patterns" by Andrew W. Krone et al.; and Serial No. 09/035,175, entitled "Direct Digital Access Arrangement Circuitry and Method for Connecting to Phone Lines" Jeffrey W. Scott et al., are expressly incorporated herein by reference.

On page 29, please replace the paragraph beginning "A preferred embodiment" with the following paragraph:

A preferred embodiment of frequency detector 818 is shown in Figure 10. The inputs to frequency detector 818 are the DATA and CK4 signals and the outputs are the SPEED-UP2 and SLOW-DOWN2 signals. Delay cell 880 has its input connected to CK4 and output connected to one input of NOR gate 882. The delay cell 880 consists of an even number of capacitively loaded inverter stages or other delay generating circuitry and is well known in the art. The output of inverter 884 is connected to the other input of NOR gate 882 and the input of inverter 884 is connected to CK4. The output 886 of NOR gate 882 is reset pulse that occurs on the rising edge of CK4, and is connected to the reset input of D flip-flops 888, 890, and 892. The input of inverter 895 is connected to DATA. The output of inverter 895 is connected to the clock input of D flip-flops 888, 890, and 892. The D input of flip-flop 888 is connected to V_{DD}. The D-input of flip-flop 890 is connected to the Q-output of flip-flop 888. The D-input of flip-flop 892 is connected to the Q-output of flip-flop 890. D flip-flops 894 and 896 have their clock

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